REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants have amended independent claims 1 and 18-21 to recite that a temperature of the semiconductor substrate during the plasma etching treatment ranges from 100° -130°. See previously considered claim 8. In light of amendments to these independent claims, claim 8 has been cancelled without prejudice or disclaimer. Claim 20 has been amended to recite a flow rate of the etching gas of 700 cm^3/minute "or over", consistent with claim 21. Moreover, independent claims 22 and 37-40 have been amended to recite that the silicon oxide insulating film is deposited over a patterned silicon nitride film with a "doped polycrystalline" silicon plug over a semiconductor substrate. Note, for example, pages 66 and 67 of Applicants' specification, and in particular the discussion by the Examiner in the second paragraph of Item 2, on page 2 of the Office Action mailed June 10, 2003.

Initially, Applicants respectfully request that the present amendments be entered. Noting amendments to claims 22 and 37-40, clearly these amendments do not raise any new issue, including any issue of new matter, the Examiner indicating in the second paragraph of Item 2 on page 2 of the Office Action mailed June 10, 2003, that pages 66 and 67 of Applicants' specification disclose a plug of doped polysilicon. Noting this comment by the Examiner in the second paragraph of Item 2, on page 2 of the Office Action mailed June 10, 2003, it is respectfully submitted that the present amendments to claims 22 and 37-30 materially limit issues remaining in connection with the above-identified application; and, at the very least,

present the claims in better form for appeal. As the present response is the first response after the indication by the Examiner in the second paragraph on page 2 of the Office Action mailed June 10, 2003, it is respectfully submitted that the present amendments are clearly timely. Moreover, noting previously considered claim 8, it is respectfully submitted that the present amendments to claims 1 and 18-21 do not raise any issues, including any issue of new matter; materially limit issues remaining in connection with the above-identified application, at the very least presenting the claims in better form for appeal; and are timely, particularly in light of contentions made by the Examiner in the Office Action mailed June 10, 2003.

In view of all the foregoing, it is respectfully submitted that Applicants have made the necessary showing under 37 C.F.R. §1.116(c); and that, accordingly, entry of the present amendments is clearly proper.

The rejection of claims 22-40 under the first paragraph of 35 U.S.C. §112, set forth in Item 2 on page 2 of the Office Action mailed June 10, 2003, is noted. Claims 22 and 37-40 have been amended to recite a "doped polycrystalline" silicon plug, in order to facilitate proceedings in connection with the above-identified application. Noting the comments by the Examiner in the second paragraph of Item 2 on page 2 of the Office Action mailed June 10, 2003, it is respectfully submitted that the rejection under the first paragraph of 35 U.S.C. §112 is moot.

Applicants respectfully submit that all claims presently in the application patentably distinguish over the teachings of the reference applied by the Examiner in the Office Action mailed June 10, 2002, that is, the

teachings of U.S. Patent No. 6,159,862 to Yamada, et al., under the provisions of 35 U.S.C. §103.

Initially, Applicants note the reference by the Examiner to the teachings of each of U.S. Patent No. 6,238,588 to Collins, et al., No. 5,282,925 to Jeng, et al., and No. 6,238,937 to Toprac, et al., in the paragraph bridging pages 3 and 4 of the Office Action mailed June 10, 2003. Each of these references is referred to in connection with the prior art rejection, while not being made a part of the formal statement of the rejection; and, more importantly, without satisfying all requirements of 35 U.S.C. §103 in connection therewith. Clearly, such reference to these three references, without referring to these references in the formal statement of the rejection, and, more importantly, without satisfying requirements of 35 U.S.C. §103 in connection therewith (e.g., showing motivation for using the teachings thereof in connection with the teachings of Yamada, et al.), is clearly improper. See In re Hoch, 166 USPQ 406, 407 n.3 (CCPA 1970).

It is respectfully submitted that if the Examiner intends to rely on these three references in any manner whatsoever, the Examiner must use these references in the formal statement of the rejection, and satisfy all requirements of 35 U.S.C. §103 in connection with combination of teachings of the applied references.

In any event, it is respectfully submitted that the teachings of the applied reference, Yamada, et al., even as applied by the Examiner (e.g., in light of teachings of the above-referred-to three U.S. patents), would have neither taught nor would have suggested such a fabrication method of a semiconductor integrated circuit device as in the present claims, including the

depositing of the silicon nitride insulating film and silicon oxide insulating film and plasma etching using the recited etching gas, and wherein a temperature of the semiconductor substrate during the plasma etching treatment ranges from 100° - 130°C. See claim 1; note also claims 18-21.

More specifically, it is respectfully submitted that the applied reference would have neither disclosed nor would have suggested such fabrication method as in the present claims, including the temperature of the semiconductor substrate as discussed previously, and moreover wherein the residence time of the etching gas within an etching chamber is set at 50-700 ms (note claim 1), more particularly 50-350 ms (see claim 18), even more particularly 100-200 ms (see claim 19); or wherein a pressure within the etching chamber during the plasma etching treatment ranges from 0.7 to 7 Pa, with a total flow rate of the etching gas passed into the etching chamber being 700 cm^3/minute or over (see claim 20), more particularly wherein a pressure within the etching chamber during the plasma etching ranges from 1.3 to 4 Pa, with a total flow rate of the etching gas passed into the etching chamber being at 700 cm^3/minute or over (see claim 21).

Furthermore, it is respectfully submitted that the reference as applied by the Examiner would have neither taught nor would have suggested such a fabrication method as in the present claims, including the depositing of a silicon oxide insulating film over a patterned silicon nitride film with a doped polycrystalline silicon plug over a semiconductor substrate; and, after forming a hard mask over the insulating film, subjecting the substrate to a plasma etching treatment using a specified etching gas so as to form a hole in the silicon oxide insulating film down to the patterned silicon nitride film in such a

manner that an upper surface of the doped polycrystalline silicon plug is exposed (see claims 22 and 37-40).

More particularly, it is respectfully submitted that these references would have neither taught nor would have suggested such a fabrication method as in the present claims, including the deposition and etching of structure over a patterned silicon nitride film with a doped polycrystalline silicon plug over a semiconductor substrate, and including the subjecting of the semiconductor substrate to a plasma etching treatment so as to form a hole in the silicon oxide insulating film down to the patterned silicon nitride film in such a manner that an upper surface of the doped polycrystalline silicon plug is exposed, and wherein a residence time of the etching gas within the etching chamber is set at 50-700 ms (see claim 22), more particularly, wherein the resident time is set at 50-350 ms (see claim 37), even more particularly 100-200 ms (see claim 38); or wherein a pressure within the etching chamber during the plasma etching ranges from 0.7 to 7 Pa and the total flow rate of the etching gas passed into the etching chamber is 700 cm^3/minute or over (see claim 39), more particularly wherein a pressure within the etching chamber during the plasma etching ranges from 1.3-4 Pa, with a total flow rate of the etching gas passed into the etching chamber being 700 cm^3/minute or over (see claim 40).

In addition, it is respectfully submitted that the teachings of the applied prior art would have neither disclosed nor would have suggested such method as in the present claim, including features as discussed previously in connection with claim 1, and including additional aspects as set forth in remaining, dependent claims, dependent ultimately on claim 1, and further

including (but not limited to) wherein the pressure during the plasma etching treatment ranges from 0.7-7 Pa (see claim 2); and/or wherein a total flow rate of the etching gas passed into the etching chamber ranges from 200-1000cm^3/minute (see claim 3), or wherein a total flow rate of the etching gas passed into the etching chamber is at 700 cm^3/minute or over (see claims 4 and 5), with a pressure within the etching chamber during the plasma etching ranging from 1.3-4 Pa (see claim 5), or wherein a flow rate of the dilution gas of the etching gas is larger than the flow rates of the fluorocarbon gas and oxygen of the etching gas (see claim 6); and/or plasma density as in claims 9 and 10; and/or wherein the fluorocarbon gas, of the etching gas, is made of C_5F_8 with the dilution gas being argon (see claim 11), a flow rate of the argon gas being as set forth in claims 12 and 13, a ratio in flow rate between the oxygen and C_5F_8 being as set forth in claims 14 and 15, and a partial pressure of C_5F_8 being that set forth in claims 16 and 17.

Furthermore, it is respectfully submitted that the applied reference would have neither taught nor would have suggested such a fabrication method of a semiconductor integrated circuit device as in the present claims, having features as discussed previously in connection with claim 22, and having additional features as set forth in dependent claims which are dependent ultimately on claim 22, including (but not limited to) a pressure within the etching chamber during the plasma etching as set forth in claim 23, or a total flow rate of the etching gas as in claims 24 and 25; and/or a pressure within the etching chamber and total flow rate of the etching gas as in claim 26; and/or wherein a flow rate of the dilution gas is larger than the flow rates of the fluorocarbon gas and oxygen, as in claim 27; and/or plasma

density during the plasma etching as in claims 28 and 29; and/or wherein the fluorocarbon gas of the etching gas is made of C_5F_8, the dilution gas being made of argon (see claim 30), with a flow rate of the argon gas as in claims 30 and 31, or a ratio in flow rate between the oxygen and C_5F_8 of the etching gas as set forth in claims 33 and 34; and/or partial pressure of C_5F_8 as in claims 35 and 36.

The present invention is directed to a method of fabricating a semiconductor integrated circuit device, particularly effective in a process forming a self-aligned contact (SAC) or a high aspect ratio contact (HARC) to, e.g., a doped polycrystalline silicon plug, in fabricating semiconductor integrated circuit devices.

As described on page 1 of Applicants' specification, there has been disclosed a technique wherein a silicon oxide layer is etched while ensuring great selectivity to a silicon nitride layer, using perfluorocycloolefins (for example, containing C_5F_8) as an etching gas.

However, as a tendency toward a high aspect ratio increases as the designed rule of integrated circuit manufacture is scaled down, it has become necessary to improve an ease-in-etching property, and also improve selectivity ratio of etching silicon oxide to silicon nitride. As described on page 3 of Applicants' specification, in the techniques of the SAC process and HARC process, where the aspect ratio (depth/width) of a hole or groove is increased, Applicants have found that there arises a problem in improving both the ease-in-etching property and etching selectivity of silicon oxide to silicon nitride. For example, where etching is carried out to enhance the ease-in-etching property of the silicon oxide film, to make a hole or groove,

the selectivity ratio between the silicon oxide film and the silicon nitride film cannot be ensured, so that a margin for short-circuiting between a conductor film buried in a hole or groove and an underlying conductor film becomes insufficient, thereby causing these films to be short-circuited. Note, in particular, the second full paragraph on page 3 of Applicants' specification.

Against this background, Applicants provide a method wherein both ease-in-etching property of the silicon oxide film and selectivity ratio of etching the silicon oxide film relative to a silicon nitride film, can be improved, in, illustratively, the SAC process or HARC process. Such improvement is achieved even in forming high aspect ratio structures. Applicants have found that the objective of both satisfactory ease-in-etching and selectivity can be achieved, where the etching is carried out in such a state that a residence time within an etching chamber is controlled to a specific range where selectivity to the silicon nitride insulating film is improved, and that this control is achieved by establishing a low pressure within the chamber and passing the etching gas at a large flow rate. That is, the oxide film is etched in a relatively short time, while establishing conditions including, for example, a low pressure and a great flow rate of an inert gas, together with a specific temperature of the substrate (e.g., semiconductor wafer) being etched, so that a good ease-in-etching property and high silicon oxide/silicon nitride selectivity ratio can be simultaneously realized.

In particular, the present invention includes an increased temperature of the semiconductor wafer during the plasma etching treatment, which increases the nitride selection ratio. This feature has been found by Applicants, as described in the paragraph bridging pages 43 and 44 of

Applicants' specification. By utilizing the relatively high temperature, a very high etching selectivity of silicon oxide over silicon nitride, while obtaining a vertical hole shape, is achieved.

As described on page 44 of Applicants' specification, conventionally the wafer temperature has been kept relatively low, in order to avoid deterioration of the SiO_2 etching characteristics at the bottom of the hole. In contrast, Applicants have found that various advantages are achieved using relatively high temperature for the wafer temperature, without introducing disadvantages, thereby achieving various advantages according to the present invention.

Furthermore, Applicants have found that according to the present invention a method can be used at later processing steps of the semiconductor integrated circuit device manufacturing process, for example, for exposing via a contact hole the upper surface of a doped polycrystalline silicon plug, with a very high etching selectivity of silicon oxide over silicon nitride and silicon. See pages 66 and 67 of Applicants' specification.

It is emphasized that according to the present invention, Applicants have found that when the temperature of the wafer being etched is raised under conditions for a low pressure and large flow rate of the inert gas, for example, the temperature being raised to a relatively high temperature of, e.g., 100°-130°C, a good ease-in-etching property and high selectivity ratio can be achieved. Note, in particular, Items (1) and (2) on each of pages 77 and 79 of Applicants' specification.

Yamada, et al. discloses a method and system for processing a substrate in the presence of high purity C_5F_8. According to an embodiment

disclosed in Yamada, et al., a gas mixture is introduced into a hermetic treatment chamber that houses a substrate having an SiO_2 layer above an SiN_x layer. The process etches the SiO_2 layer using a gas mixture that includes at least C_5F_8 and CO until the SiN_x layer is exposed, and subsequently etches the SiO_2 layer using C_5F_8 and at least on of CO and O_2 after the SiN_x has been exposed. See column 4, lines 54-61. Note also the paragraph bridging columns 4 and 5 of this patent. As seen in Fig. 2 of Yamada, et al., arrival of etching ions (fluorine radicals) at the silicon nitride film 206 is inhibited, and since the SiN_x film 206 can be protected, selection ratio between the SiN_x film 206 and the SiO_2 film 208 can be improved. This patent discloses a photoresist 212 which serves as a mask for the contact hole 210, formed above the SiO_2 film 208. See column 8, line 17-32. Note also column 8, lines 33-37. This patent also describes, in connection with Figs. 3A and 3B, use of the gas mixture of C_5F_8 and CO to etch a substrate. Note column 8, lines 49-55, describing the temperature of the lower electrode being maintained at 40°C.

It is respectfully submitted that Yamada, et al., discloses a procedure performed at conventionally, relatively low temperatures of, for example, 40°C. It is respectfully submitted that this patent does not disclose, nor would have suggested, a method as in the present claims, including the temperature of the substrate during the etching, of 100°-130°C, and advantages thereof. Thus, emphasizing the relatively low temperatures in Yamada, et al., it is respectfully submitted that this patent would have taught away from the present invention, including temperature of the substrate during processing, and advantages thereof.

The comments by the Examiner in connection with the teachings of Yamada, et al., in the first full paragraph on page 5 of the Office Action mailed June 10, 2003, is noted. The Examiner acknowledges that Yamada, et al., "does not disclose the temperature of the substrate being plasma etched in its process". The Examiner goes on to state, however, that the temperature of the substrate is commonly determined by routine experimentation, and that it would have been obvious to one of ordinary skill in the art to optimize the temperature through routine experimentation in order to produce an expected result. However, it is respectfully submitted that Yamada, et al., discloses a specific temperature of a treatment, much lower than that according to the present invention. In addition, the present disclosure provides advantages achieved by the present invention, including the relatively high temperature. Particularly since Yamada, et al., teaches away from the relatively high temperature as in the present claims, it is respectfully submitted that the Examiner errs in connection with the conclusion concerning routine experimentation. To the contrary, it is respectfully submitted that Applicants have utilized a temperature neither disclosed nor suggested by the prior art, and achieves an unexpectedly better result therefrom, as discussed in the foregoing.

The additional contention by the Examiner that any changes in temperature different from that in Yamada, et al., "do not impart patentability unless the recited ranges are critical" is respectfully traversed. Initially, it is respectfully submitted that Applicants have shown unexpectedly better advantages achieved by the present relatively high temperature, thus even satisfying the criterion set forth by the Examiner.

Moreover, it is respectfully submitted that Yamada, et al., disclosing specific low temperatures during the etching, teaches away from the process as presently claimed including temperature of the semiconductor substrate during the plasma etching treatment; it is respectfully submitted that, particularly in view of the teachings of Yamada, et al., as a whole, all of which must be considered by the Examiner in a determination of obviousness under 35 U.S.C. §103, the disclosure of this patent would have taught away from the present invention, such that the determination of temperature as in the present claims is not a determination of an optimum range obtained through routine experimentation.

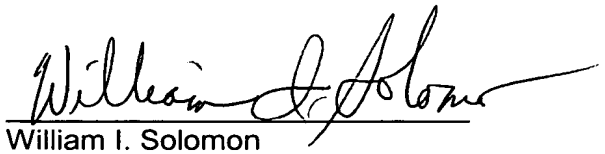
Moreover, Yamada, et al., is clear in connection with forming a hole through to a silicon nitride film on a silicon substrate (that is, wafer) 200. The disclosure would have neither taught nor would have suggested the method including forming the contact hole exposing the doped polycrystalline silicon plug, that is, a subsequent processing step in the manufacture of the semiconductor device than the disclosed in Yamada, et al., as applied by the Examiner, and advantages thereof as discussed in the foregoing.

In view of the foregoing comments and amendments, reconsideration and allowance of all claims remaining in the application are respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to

Deposit Account No. 01-2135 (Case No. 501.40201X00) and please credit any excess fees to such deposit account.

Respectfully submitted,



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